Customer No.: 31561
Application No.: 10/605,011
Docket NO.: 10874-US-PA

AMENDMENT

In the Claims:

Claim 1. (original) A verifying apparatus for a liquid crystal driving circuit having a plurality of driving stages, comprising:

a storage unit for receiving and storing a first trigger pulse during a first time period and receiving and storing a second trigger pulse during a second time period, and then sequentially outputting a first shifted signal and a second shifted signal that correspond to the stored first and second trigger pulse;

a first data switch electrically coupled to the output terminal of the storage unit so that the output terminal of the first data switch is electrically connected to a first output path during the first time period and the output terminal of the first data switch is electrically connected to a second output path during the second time period; and

an edge detector having an input terminal electrically connected to the first output path and an output terminal electrically connected to the second output path, wherein if no edge transition is detected during the first time period, the second output path is set to a pre-defined logic potential during the second time period.

Claim 2. (original) The verifying apparatus of claim 1, wherein the apparatus furthermore comprises a second data switch having an output terminal that serves as an input terminal to the storage unit, an input terminal electrically connected to the output terminal of a driving stage two driving stages before for receiving the first trigger pulse and a second input terminal electrically connected to the output terminal of a driving stage one driving stage before for receiving the second trigger pulse.

Claim 3. (original) The verifying apparatus of claim 1, wherein the storage unit comprises a shift register.

Claim 4. (original) A liquid crystal display driving circuit having a plurality of driving stages with each driving stage comprising:

a plurality of verifying apparatus with each verifying apparatus having:

a storage unit for receiving and storing a first trigger pulse during a first time period and receiving and storing a second trigger pulse during a second time period, and then sequentially outputting a first shifted signal and a second shifted signal that correspond to the stored first and second trigger pulse;

a first data switch electrically coupled to the output terminal of the storage unit so that the output terminal of the first data switch is electrically connected to a first output path during the first time period and the output terminal of the first data switch is electrically connected to a second output path during the second time period;

an edge detector having an input terminal electrically connected to the first output path and an output terminal electrically connected to the second output path, wherein if no edge transition is detected during the first time period, the second output path is set to a pre-defined logic potential during the second time period;

a logic operation unit with a receiving terminal electrically connected to the second output path of various verifying apparatus for executing a corresponding logic operation according to the pre-defined logic potential so that the output from the logic operation unit is unaffected by the pre-defined logic potential; and

a driving switch for cutting off the electrical connection of the driving

stage with a pixel circuit during a first time period but reconnecting with the pixel circuit during the second time period.

Claim 5. (original) The liquid crystal display driving circuit of claim 4, wherein the logic operation unit executes a logic 'AND' operation when the pre-defined logic potential is at a logic level '1'.

Claim 6. (original) The liquid crystal display driving circuit of claim 4, wherein the logic operation unit executes a logic 'OR' operation when the pre-defined logic potential is at a logic level '0'.

Claim 7. (original) The liquid crystal display driving circuit of claim 4, wherein each verifying apparatus furthermore comprises a second data switch having an output terminal that serves as an input terminal to the storage unit, an input terminal electrically connected to the output terminal of a driving stage two driving stages before for receiving the first trigger pulse and a second input terminal electrically connected to the output terminal of a driving stage one driving stage before for receiving the second trigger pulse.

Claim 8. (original) The liquid crystal display driving circuit of claim 4, wherein the number of verifying apparatus inside the display is two.

Claim 9. (original) The liquid crystal display driving circuit of claim 4, wherein the storage unit comprises a shift register.

Claim 10. (cancelled).

Claim 11. (original) An error tolerance method for a liquid crystal display driving circuit having a driving circuit with a plurality of verifying apparatus therein, wherein each verifying apparatus comprises a storage unit for holding driving signals, the error

tolerance method comprising the steps of:

receiving a pre-determined trigger pulse;

checking to determine if the trigger pulse transmitted via the storage unit is normal or not;

setting the output terminal of the verifying apparatus to a pre-defined logic potential if the trigger pulse transmitted from the storage unit is found to be abnormal; and

executing a logic operation that correspond to the pre-defined logic potential so that the result from the logic operation is unaffected by the pre-defined logic potential.

Claim 12. (original) The error tolerance method of claim 11, wherein the step of determining if the trigger pulse transmitted from the storage unit is normal or not comprising:

transferring the trigger pulse to the storage unit;

retrieving the trigger pulse data from the storage unit;

determining if the trigger pulse data has the same logical variation as the original trigger pulse; and

judging the transmitted trigger pulse to be normal if the trigger pulse data from the storage unit and the original trigger pulse are identical, otherwise, judging the transmitted trigger pulse to be abnormal.

Claim 13. (original) The error tolerance method of claim 11, wherein the logic operation is an 'AND' operation when the pre-defined logic potential is at a logic level '1'.

Claim 14. (original) The error tolerance method of claim 11, wherein the logic operation is an 'OR) operation when the pre-defined logic potential is at a logic level '0'.